

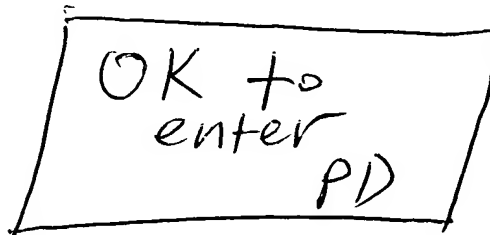


IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Attila Kovacs and Jeffrey A. Buckles  
Assignee: NEC Electronics America, Inc.  
Title: SYSTEM AND METHOD FOR REDUCING TIMING VIOLATIONS  
DUE TO CROSSTALK IN AN INTEGRATED CIRCUIT DESIGN  
Application No.: 10/650,010 Filing Date: August 27, 2003  
Examiner: Paul Dinh Group Art Unit: 2825  
Docket No.: NEC0255US Confirmation No.: 6058

Austin, Texas  
February 22, 2005

MAIL STOP AF  
COMMISSIONER FOR PATENTS  
P. O. BOX 1450  
ALEXANDRIA, VA 22313-1450



RESPONSE TO FINAL OFFICE ACTION

Dear Sir:

This paper is responsive to the Office Action dated November 22, 2005, having a shortened statutory period expiring on February 22, 2006. Further examination and reconsideration are respectfully requested in view of the amendments and remarks set forth below.

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

No Amendments to the Drawings are presented in this paper.

Remarks begin on page 13 of this paper.